Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 1 – 62 remain.

Claims 1 – 34 have been cancelled.

Claims 35 and 54 are being amended.

WHAT IS CLAIMED IS:

1 – 34 (Cancelled)

35. (Currently Amended) A data converter, comprising:

a duty cycle modulator for converting a received data stream having a sampling frequency into a duty cycle modulated data stream having a duty cycle modulation frequency; and

a finite impulse response filter <u>responsive to the duty cycle modulated data stream and having a transfer function</u> for attenuating <u>at</u> multiples of the duty cycle modulation frequency [[from]] the duty cycle modulated data stream.

36. (Original) The data converter of Claim 35, wherein the finite impulse response filter has a null at the duty cycle modulation frequency.

37. (Original) The data converter of Claim 35, further comprising a plurality of digital to analog conversion elements coupled to corresponding taps of the finite impulse response filter.

38. (Original) The data converter of Claim 37, wherein the plurality of digital to analog conversion elements comprise continuous time conversion elements.

39. (Original) The data converter of Claim 38, wherein the conversion elements comprise controlled current sources.

40. (Original) The data converter of Claim 38, wherein the conversion elements comprise resistors.

41. (Original) The data converter of Claim 35, further comprising:

a second duty cycle modulator for converting a second data stream having a second sampling frequency into a second duty cycle modulated data stream having a second duty cycle modulation frequency; and

a second finite impulse response filter for attenuating multiples of the second duty cycle modulation frequency.

42. (Original) The data converter of Claim 41, wherein the second duty cycle modulation frequency is the same as the duty cycle modulation frequency.

43. (Original) The data converter of Claim 41, further comprising combining circuitry for combining outputs of the first and second filters.

44. (Original) The data converter of Claim 41, further comprising de-interleaving circuitry for de-interleaving an input data stream into the received data stream and the second data stream.

45. (Original) The data converter of Claim 35, further comprising a delta-sigma modulator for noise shaping the input data stream, wherein the delta-sigma modulator

has a noise transfer function with multiple attenuation bands for reducing noise exposure to mismatch between the duty cycle modulator and the second duty cycle modulator.

46. (Original) The data converter of Claim 35, wherein the received data stream is generated by a delta-sigma modulator having at least one integrator and non-linear feedback to the at least one integrator.

47. (Original) The data converter of Claim 35, wherein the non-linear feedback corrects for variations in a selected moment of the duty cycle modulated data stream.

48. (Original) The data converter of Claim 47, wherein the non-linear feedback is provided by a selected one of non-linear feedback operations.

49. (Original) A digital to analog converter, comprising:

a noise shaper for generating a noise-shaped data stream at a first sampling frequency;

at least one pulse width modulator stage for generating from the noise-shaped data stream a pulse width encoded data stream at a second sampling frequency of a selected multiple of the first sampling frequency;

output circuitry for converting the pulse width encoded data stream into an analog signal comprising:

a finite impulse response filter for attenuating the pulse width encoded data stream at multiples of the first sampling frequency; and

a plurality of digital to analog conversion elements coupled to selected taps of the finite impulse response filter for generating an output analog signal.

50. (Original) The digital to analog converter of Claim 49, wherein the noise shaper comprises a delta-sigma modulator having a plurality of integration stages and

correction circuitry for selectively feeding back correction factors to selected ones of the integration stages for correcting for variations in a moment of the pulse width encoded stream.

51. (Original) The digital to analog converter of Claim 50, wherein the at least one pulse width modulation stage comprises a plurality of parallel pulse width modulation stages, wherein the digital to analog converter further de-interleaves the noise shaped data stream into a plurality of data streams corresponding to the plurality of pulse width modulation stages and each of the plurality of data streams has a sampling frequency proportional to the first sampling frequency of the noise shaped data stream and a number of the plurality of pulse width modulation stages.

52. (Original) The digital to analog converter of Claim 51, wherein the noise shaper comprises a delta-sigma modulator with multiple noise attenuation bands in an output noise transfer function for reducing noise exposure to mismatch between the plurality of pulse width modulation stages.

53. (Original) The digital to analog converter of Claim 49, wherein the plurality of digital to analog conversion elements comprises a plurality of continuous-time digital to analog conversion elements.

54. (Currently Amended) A method of data conversion, comprising:

converting a data stream having a sampling frequency into a duty cycle modulated data stream having a duty cycle modulation frequency; and

attenuating multiples of the duty cycle modulation frequency of the duty cycle modulated data stream with a finite impulse response filter <u>having a corresponding transfer function</u>.

55. (Original) The method of Claim 54, further comprising noise shaping the data stream to conversion into the duty cycle modulated data stream.

56. (Original) The method of Claim 54, wherein attenuating comprises filtering the stream of duty cycle modulated data with a finite impulse filter having a null at the duty cycle modulation frequency.

57. (Original) A duty cycle modulation system comprising:

a duty cycle modulator receiving a first data stream sampled at a first sampling frequency and outputting a second data stream sampled at a second sampling frequency;

a finite impulse response filter for selectively filtering the second data stream.

58. (Original) The duty cycle modulation system of Claim 57, wherein the finite impulse response filter attenuates signals generated by the duty cycle modulator.

59. (Original) The duty cycle modulation system of Claim 57, wherein second sampling frequency is an integer multiple of the first sampling frequency.

60. (Original) The duty cycle modulation system of Claim 57, wherein the second sampling frequency is a fractional multiple of the first sampling frequency.

61. (Original) The duty cycle modulation system of Claim 57, wherein the finite impulse response filter attenuates frequencies above the first sampling frequency.

62. (Original) The duty cycle modulation system of Claim 57, wherein the finite impulse response filter has low pass filter characteristics.